

Notice of References Cited	Application/Control No. 10/726,902		Applicant(s)/Patent Under Reexamination ALSUP ET AL.	
	Examiner Robert E. Fennema		Art Unit 2183	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
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*	B	US-3,896,419	07-1975	Lange et al.	711/129
*	C	US-2004/0143721	07-2004	Pickett et al.	711/217
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	K	US-			
	L	US-			
	M	US-			

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NON-PATENT DOCUMENTS

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	U	Rotenberg et al. "Trace Cache: A Low Latency Approach to High Bandwidth Instruction Fetching". Published in the Proceedings of the 29th Annual International Symposium on Microarchitecture, Dec 2-4, 1996. Pages 24-35.
	V	Brought, Grant. "Class #21 - Assemblers, Labels & Pseudo Instructions". November 16, 2000.
	W	Patterson, David. Hennessy, John. "Computer Architecture: A Quantitative Approach". Morgan Kaufmann Publishers, Inc, 2nd Edition, 1996. Pages 271-278.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.